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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/526,957	03/16/2000	Robert David Sebesta	EN9-98-141	1611

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 09/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/526,957	SEBESTA ET AL.84	
	Examiner	Art Unit	
	James Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-13 and 27-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-13 and 27-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2-7, 9-13 and 27-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With respect to claims 2 and 3, it is unclear how circuit lines can be "totally external *aside* from being in contact with substrate." The sentence with the word **aside,** in scope, includes an area of the line that is in the substrate and therefore not "totally external" form the substrate.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2-4,11, 33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsusaka et al (U.S 4,959,510).

5. Matsusaka (Fig 1-3) discloses an electronic structure comprising: a substrate (11), a first circuit line (a portion of 4 that defines a line) including an inherent first conductive pad (region of line in contact with bump) and having a first thickness extending in a direction perpendicular to a surface of the substrate at which the first

circuit line is coupled to the substrate, and wherein the first circuit line is inherently totally external to the substrate aside from being in contact with the substrate ("on substrate"; Column 2, Lines 47-49) and a second circuit line (2b) including an inherent second conductive pad and having a second thickness extending in a direction perpendicular to a surface of the substrate at which the second circuit line is coupled to the substrate, wherein the second circuit line is electrically coupled the first signal line (via chip) and a thickness of the second circuit line is unequal to the first thickness, wherein the second circuit line is inherently totally external to the substrate aside from being in contact with the substrate ("on substrate"; Column 2, Lines 47-49), and the first line is in direct mechanical contact with the second circuit line (Column 2, Lines 39-42); wherein an end of the first circuit line includes a conductive pad and the end of the second circuit line includes a conductive pad; wherein the first conductive pad includes a metallic layer (12), and further comprising a first metallic coating (13) over the metallic layer and a second metallic coating over the first (14) wherein the first metallic coating inhibits diffusion of a metal from the second metallic coating into the metallic layer; a third circuit line (3) having a thickness that is unequal to the first and second thickness, and wherein the third line is inherently electrically coupled and in direct mechanical contact to the first line (third line forms a part of first line) and is electrically and in direct mechanical contact to the second circuit line (via soldering of chip, 5a).

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 2, 6, 7 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Murakami et al (U.S 6,031,292).

8. Murakami (Fig 1-3) discloses an electronic structure comprising: a substrate (1), a first circuit line including an inherent conductive pad (3) and having a first thickness extending in a direction perpendicular to a surface of the substrate at which the first circuit line is coupled to the substrate, and wherein the first circuit line is totally external to the substrate aside from being in contact with the substrate, and a second circuit line (6) including a second inherent conductive pad and having a second thickness extending in a direction perpendicular to a surface of the substrate at which the second circuit line is coupled to the substrate, wherein the second circuit line is electrically coupled the first signal line via the first circuit line is coupled a first end of a plated through hole (5) and a second circuit line is coupled to a second end of the PTH, wherein a thickness of the second circuit line is unequal to the first thickness, wherein the second circuit line is totally external to the substrate aside from being in contact with the substrate, and the first line is inherently in direct mechanical contact with the second circuit line (via Plated Through Hole); wherein the first circuit line is coupled to a top

surface of the substrate and the second circuit line is coupled to a bottom surface of the substrate.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

11. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsusaka as applied to claims 2 and further in combination with Frey et al. (U.S 5,249,101).

13. Frey utilizes a protective coating (Lines 49-54, Column 3). It would have been obvious to combine Matsusaka's circuit patterns with Frey's protective coating in order to protect the circuitry from mechanical and environmental hazards.

14. Claim 12, 13 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsusaka as applied to claims 3 and 11 and further in combination with Lee et al. (U.S 6,050,832) and Lan et al. (U.S 5,767,575).

15. Matsusaka further discloses a solder ball (51) coupled to the second conductive pad (2b), an electronic assembly ("chip", 6a) and a first metallic coating consisting of nickel and a second metallic coating consisting of gold.

16. Matsusaka does not appear to explicitly disclose an electronic assembly coupled to a wirebond interconnect that is coupled to the first conductive pad (4) at the second metallic coating, an electronic carrier coupled to a solder ball coupled to the second conductive pad or that the metallic layer includes copper.

17. Lee utilizes an interposer (218) that carries a chip and therefore is a carrier.

18. It would have been obvious to one of ordinary skill in the art to incorporate an electronic carrier between the chip and substrate such that it is coupled to the solder ball (51, 52) in order to reduce thermal stresses as taught by Lee (Abstract).

19. In regards to the electronic assembly (6a) having a wirebond interconnect, the prior art discloses a flip chip connection instead of a wirebond, Lan (Column 1, Lines 42-47) shows that wirebond is an equivalent structure known in the art. Therefore, because these two interconnections were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a flip chip for a wirebond.

20. With respect to the metallic layer being copper, it would have been obvious to one of ordinary skill in the art to form the circuit line of copper in order provide good

electrical properties, since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter o f obvious design choice. *In re Leshin*, 125 USPQ 416 (1960).

21. Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami as applied to claims 2 and 6 and further in combination with Sherman (U.S 5,784,262).

22. Murakami does not show a first solder ball coupled to the first conductive pad an electronic assembly coupled to the first solder ball with a second solder ball coupled to the second conductive pad with an electronic carrier coupled to the second solder ball.

23. However Sherman utilizes a first solder ball (16A) coupled to a first conductive pad and an electronic assembly (10) coupled to the first solder ball.

24. It would have been obvious to one of ordinary skill in the art to modify the electronic assembly interconnect of Murakami by coupling the electronic assembly to the first bond pad by a first solder ball in order to provide increased density as taught by Sherman Column 1, Lines 30-33).

25. Claims 10 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami and Sherman as applied to claim 9 and further in combination with Tamaoki (JP 02-43748).

26. Neither Murakami or Sherman disclose that the diameter of the second solder ball is unequal to a diameter of the first solder ball, however Tamaoki (Fig 2) utilizes a second solder ball (14) with a diameter unequal to a diameter of a first solder ball (15).

27. It would have been obvious to one of ordinary skill in the art to form a second solder ball with a diameter to unequal to a diameter of a first solder ball in order to mount the smaller ball on the smaller circuit line without bonding defects as taught by Tamaoki (English Abstract).

28. Claims 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami as applied to claim 6 and further in combination with Sambucetti (U.S 6,355, 104).

29. Murakami further discloses a wirebond interconnect (7) coupled to the first conductive pad, and an electronic assembly (2) coupled to the wirebond interconnect, a solderball coupled to the second conductive pad, and a carrier (8) coupled to the solder ball.

30. Murakami does not appear to disclose said pad including a copper metallic coating with a first metallic coating including nickel over the copper and a second metallic coating including gold or palladium over the first metallic coating that includes nickel wherein the wirebond interconnect is a gold.

31. Sambucetti (Fig 1) utilizes a pad including a copper metallic coating (12) with a first metallic coating including nickel (16) over the copper and a second metallic coating including gold (18) over the first metallic coating that includes nickel with a wirebond interconnect of gold.

32. It would have been obvious to one of ordinary skill in the art to form the pad of copper to provide an electrical contact and to form a first metallic coating including nickel (16) over the copper and a second metallic coating (18) over the first metallic

coating that includes nickel with a wirebond interconnect of gold in order to eliminate pad lift-off as taught by Sambucetti (Column 1, Lines 32-34; Column 2, Lines 15-19).

Response to Arguments

33. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection and applicant's subsequent amendment to the claims filed July 25, 2002, thereby eliminating the negative limitation of "the circuit line being not embedded in the substrate."

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
September 12, 2002

DAVID E. GRAYBILL
PRIMARY EXAMINER